16. The device, as defined in claim 14, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

17. The device, as defined in claim 14, wherein a plurality of dummy gates are commonly connected on the substrate.

18. (Twice Amended) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate is of predetermined width and length at a substantially identical gap therebetween without intervening dummy gates therebetween; and

a plurality of dummy gates having predetermined width and length between and outside ones of the adjacent transistors at a substantially identical gap therebetween, without intervening transistor gates therebetween, respectively.

19. The device, as defined in claim 18, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

20. The device, as defined in claim 18, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

21. The device, as defined in claim 18, wherein a plurality of dummy gates are commonly connected on the substrate.

22. (Twice Amended) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate has a predetermined width and length at a substantially identical gap therebetween without intervening dummy gates therebetween; and

a plurality of dummy gates having predetermined width and length outside ones of the adjacent transistors at a substantially identical gap therebetween, without intervening transistor gates therebetween, respectively.

23. The device, as defined in claim 22, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

24. The device, as defined in claim 22, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

25. The device, as defined in claim 22, wherein a plurality of dummy gates are commonly connected on the substrate.

29. (Twice Amended) A semiconductor device comprising:

a substrate;

active regions having a source region and a drain region on the substrate;

a portion other than the active region on the substrate;

a plurality of transistor gates formed on the active regions, the gates being disposed between the source region and the drain region and having a first gap between adjacent gates, without intervening dummy gates therebetween;

a plurality of dummy gates formed on the portion, the dummy gates being characterized by a second gap between adjacent dummy gates, without intervening transistor gates therebetween, respectively;

wherein the second gap is substantially identical to the first gap.

30. The device, according to claim 29, in which a first metal is connected to the source region and the drain region by a plurality of contacts.

31. The device, according to claim 30, in which a second metal is connected to a first part of the first metal to supply a voltage.

32. The device, according to claim 31, in which the plurality of dummy gates are commonly connected by a second part of the first metal to supply a ground voltage.

33. (Twice Amended) A semiconductor device comprising

a substrate;

a first region having a plurality of first active regions each having a source region and a drain region respectively and a first portion other than the plurality of first active regions on the substrate;

a second region having a plurality of second active regions each having a source region and a drain region respectively and a second portion other than the plurality of second active regions on the substrate;

a plurality of first transistor gates formed on the plurality of first active regions, disposed between the source region and the drain region, the plurality of first transistor gates being characterized by a first gap between neighboring transistor gates, without intervening transistor gates therebetween;

a plurality of second transistor gates formed on the plurality of second active regions, the plurality of second transistor gates also being characterized by the first gap between neighboring gates;

a plurality of first dummy gates formed on the first portion, the plurality of first dummy gates being characterized by a second gap between neighboring dummy gates, without intervening transistor gates therebetween;

a plurality of second dummy gates formed on the second portion, the plurality of second dummy gates also being characterized by the second gap between neighboring dummy gates without intervening transistor gates therebetween;

a first metal connected to the source and drain regions by a contact; and

a second metal connected to a first part of the first metal to supply a voltage.

34. The semiconductor device according to claim 33, in which the first gap is substantially identical to the second gap.

35. The semiconductor device according to claim 33, in which the second metal is connected to a second part of the first metal to supply a ground voltage.

36. (Amended) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, without intervening transistors therebetween, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between more than one first and second electrodes of those active regions, the plurality of transistor gates being characterized by a predetermined first dimension and a variable second dimension on the substrate; and

a plurality of dummy gates disposed on the substrate between more than one first and second electrodes of those active regions, the plurality of dummy gates being characterized by dummy gates that substantially fill the region on the substrate devoid of transistor gates in the second dimension;

wherein the plurality of transistor gates have substantially identical first and second dimensions.

37. The semiconductor device according to claim 36, in which the first dimension characterizes a transistor gate length.

38. The semiconductor device according to claim 37, in which the second dimension characterizes a transistor gate width.

39. (Amended) The semiconductor device according to claim 36, in which adjacent ones of the plurality of transistor gates and of the plurality dummy gates are of substantially identical gap between gates.

40. (New) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between more than one first and second electrodes of those active regions respectively, wherein two or more transistor gates are of an elongated length relative to width; and

a plurality of dummy gates having an elongated length relative to width and located and oriented in aligned opposition to the transistor gates.

41. (New) The semiconductor device according to claim 40, in which the plurality of transistor gates and of the plurality dummy gates are of substantially identical gap between gates.

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42. (New) The device, as defined in claim 40, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

43. (New) The device, as defined in claim 40, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

44. (New) The device, as defined in claim 40, wherein a plurality of dummy gates are commonly connected on the substrate.

45. (New) The device, as defined in claim 40, wherein the width of the dummy gates is substantially the same as that of the transistor gates.

46. (New) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between more than one first and second electrodes of those active regions respectively, wherein two or more transistor gates are of an elongated length relative to width; and

a plurality of dummy gates having a first portion in contact with a bias line and one or more second portions extending in a vertical direction and disposed on the substrate such that the one or more second portions are interspaced between adjacent transistor gates.

47. (New) The semiconductor device according to claim 46, in which the plurality of transistor gates and of the plurality dummy gates are of substantially identical gap between gates.

48. (New) The device, as defined in claim 46, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

49. (New) The device, as defined in claim 46, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

50. (New) The device, as defined in claim 46, wherein a plurality of dummy gates are commonly connected on the substrate.

51. (New) The device, as defined in claim 46, wherein the width of the dummy gates is substantially the same as that of the transistor gates.

52. (New) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between more than one first and second electrodes of those active regions respectively, wherein two or more transistor gates are of an elongated length relative to width; and

a plurality of dummy gates having an elongated length relative to width and aligned in vertical opposition to the transistor gates, the length of the dummy gates being substantially the same as that of the transistor gates;

wherein the plurality of transistor gates and the plurality of dummy gates are of substantially identical gap between gates;

and wherein the plurality of transistors and the plurality of dummy gates are commonly connected on the substrate, respectively.

53. (New) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between more than one first and second electrodes of those active regions respectively, wherein two or more gates are of an elongated length relative to width; and

a plurality of dummy gates having a first portion in contact with a bias line and one or more second portions extending in a vertical direction and disposed on the substrate such that the one or more second portions are interspaced between adjacent transistor gates, the length of the dummy gates being substantially the same as that of the transistor gates,

wherein the plurality of transistor gates and the plurality of dummy gates are of substantially identical gap between gate;

and wherein the plurality of transistors and the plurality of dummy gates are commonly connected on the substrate, respectively.

54. (New) A semiconductor device comprising:

a substrate;

a rectangular region on the substrate;

an active region having a first width and a second width on said rectangular region;

an isolation portion of said active region on said rectangular region;

first transistor gates on said first width of said active region;

second transistor gates on said second width; and

first dummy gates on said isolation portion aligned with said first transistor gates;

wherein said first width is less than said second width;

and wherein said transistor gates and said first dummy gates are of substantially identical gap between gates.

55. (New) The device of claim 54 wherein said active region is n-type.

56. (New) The device of claim 54 wherein said active region is p-type.

57. (New) The device of claim 54, further comprising:

second dummy gates on said rectangular region having a substantially identical width as said second transistor gates.

58. (New) The device of claim 57 wherein said active region is n-type.

59. (New) The device of claim 57 wherein said active region is p-type.